IN THE CLAIMS

Please amend the claims as follows. All the claims as amended are set forth.

1-46. (canceled)

47. (currently amended) A method for fabricating a microelectromechanical apparatus comprising:

forming a layer of dielectric material on a first side of the substrate;

forming on the first side of the substrate vertical isolation trenches containing dielectric material;

patterning a masking layer on a second side of the substrate that is opposite to the first side of the substrate;

forming vias on the first side of the substrate;

metallizing the first side of the substrate;

forming second trenches on the first side of the substrate to define structures;

deeply etching the second side of the substrate to form narrow blades;

after forming the narrow blades, ~~coupling~~ bonding a base wafer to the second side of the substrate;

etching through the vias on the first side of the substrate to release the structures and to provide electrical isolation, wherein at least one of the narrow blades is isolated by one of the vertical isolation trenches, and wherein at least one of the narrow blades is coupled to one of the structures.

48. (canceled)

49. (original) The method of claim 47, wherein the substrate comprises a silicon wafer.

50. (original) The method of claim 47, further comprising attaching a protective

lid to the first side of the substrate.

51. (original) The method of claim 47, wherein the dielectric material is silicon dioxide.

52. (original) The method of claim 47, further comprising depositing a second metal layer on the first side of the substrate after metallizing the first side of the substrate in order to form a reflective surface.

53. (original) The method of claim 47, further comprising forming a passivation layer on the first side of the substrate after metallizing the first side of the substrate.

54. (canceled)

55. (original) The method of claim 50, wherein the protective lid comprises glass.

56. (currently amended) A method for fabricating a microelectromechanical apparatus, comprising:

patterning a masking layer on a second side of a substrate having a first side that is opposite to the second side of the substrate;

deeply etching the second side of the substrate to form narrow blades;

after forming the narrow blades, fusion bonding a recessed base wafer to the second side of the substrate;

forming a layer of dielectric material on the first side of the substrate;

forming on the first side of the substrate vertical trenches containing dielectric material;

forming vias on the first side of the substrate;

metallizing the first side of the substrate;

forming second trenches on the first side of the substrate to define structures;

etching through the vias on the first side of the substrate to release the structures, wherein at least one of the narrow blades resides between two of the vertical trenches, and wherein at least one of the narrow blades is coupled to one of the structures.

57. (original) The method of claim 56, wherein the substrate comprises a silicon wafer.

58. (original) The method of claim 56, further comprising attaching a protective lid to the first side of the substrate.

59. (previously presented) The method of claim 56, further comprising thinning the first side of the substrate prior to forming a layer of dielectric material on the first side of the substrate.

60. (canceled)

61. (original) The method of claim 56, wherein the dielectric material is silicon dioxide.

62. (original) The method of claim 56, further comprising depositing a second metal layer on the first side of the substrate after metallizing the first side of the substrate in order to form a reflective surface.

63. (original) The method of claim 56, further comprising forming a passivation layer on the first side of the substrate after metallizing the first side of the substrate.

64. (canceled)

65. (previously amended) The method of claim 58, wherein the protective lid comprises glass.

66. (currently amended) A method for fabricating a microelectromechanical apparatus comprising:

forming a layer of dielectric material on a first side of a silicon-on-insulator (SOI) substrate;

patterning a masking layer on a second side of the SOI substrate that is opposite to the first side of the SOI substrate;

forming vias on the first side of the SOI substrate that extend through a buried oxide layer of the SOI substrate;

metallizing the first side of the SOI substrate;

forming trenches on the first side of the SOI substrate to define structures;

forming a passivation layer on the first side of the substrate on metallization of the first side of the SOI substrate and on sidewalls of the vias and trenches of the first side of the SOI substrate;

deeply etching the second side of the SOI substrate to form narrow blades, wherein at least one narrow blade is coupled to one of the structures and wherein at least one narrow blade resides beneath at least one via;

after forming the narrow blades, ~~coupling~~bonding a base wafer to the second side of the SOI substrate;

etching through the vias on the first side of the substrate to release the structures.

67. (canceled)

68. (original) The method of claim 66, wherein the SOI substrate comprises an SOI wafer.

69. (previously presented) The method of claim 66, further comprising using a frit glass seal to attach a glass protective lid to the first side of the SOI substrate.

70. (original) The method of claim 66, wherein the dielectric material is silicon dioxide.

71. (original) The method of claim 66, further comprising depositing a second metal layer on the first side of the SOI substrate after metallizing the first side of the SOI substrate in order to form a reflective surface.

72. (previously presented) The method of claim 66, wherein deeply etching the second side of the substrate to form narrow blades comprises etching to the buried oxide layer of the SOI substrate.

73-74. (canceled)

75. (currently amended) A method for fabricating a microelectromechanical apparatus, comprising:

patterning a masking layer on a second side of the substrate that is opposite to a first side of the substrate;

attaching a spacer substrate to the second side of the substrate resulting in cavities;

forming a layer of dielectric material on the first side of the substrate; forming on the first side of the substrate vertical trenches containing dielectric material;

forming vias on the first side of the substrate;

metallizing the first side of the substrate;

forming second trenches on the first side of the substrate to define structures;

etching an opening through the spacer substrate to expose the masking layer on the second side of the substrate;

deeply etching the second side of the substrate to form narrow blades;

after forming the narrow blades, ~~coupling~~bonding a base wafer to the spacer substrate;

etching through the vias on the first side of the substrate to release the structures, wherein at least one of the narrow blades resides between two of the vertical trenches, and wherein at least one of the narrow blades is coupled to one of the structures.

76. (canceled)

77. (original) The method of claim 75, wherein the substrate comprises a silicon wafer.

78. (original) The method of claim 75, further comprising attaching a protective lid to the first side of the substrate.

79. (original) The method of claim 75, wherein the dielectric material is silicon dioxide.

80. (original) The method of claim 75, further comprising depositing a second metal layer on the first side of the substrate after metallizing the first side of the substrate in order to form a reflective surface.

81. (original) The method of claim 75, further comprising forming a passivation layer on the first side of the substrate after metallizing the first side of the substrate.

82. (canceled)

83. (original) The method of claim 78, wherein the protective lid comprises glass.

84-119. (canceled)